CLAIMS:

1. Silicon-on-insulator comprising integrated circuitry, comprising:

a substrate comprising an insulator layer of silicon-on-insulator circuitry, the insulator layer comprising silicon dioxide;

a semiconductive silicon comprising layer of the silicon-on-insulator circuitry, the silicon comprising layer being received proximate the insulator layer, the silicon comprising layer comprising a pair of source/drain regions formed therein and a channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

a silicon nitride comprising region received intermediate the silicon dioxide comprising layer and the source/drain regions and running along at least a portion of the channel region between the source/drain regions.

2. The circuitry of claim 1 wherein the silicon nitride comprising region runs along only a portion of the channel region between the source/drain regions.

3. The circuitry of claim 1 wherein the silicon nitride comprising region runs entirely along the channel region between the source/drain regions.

4. The circuitry of claim 1 wherein the silicon comprising layer contacts the insulator layer, and the source/drain regions extend to the insulator layer.

5. The circuitry of claim 1 wherein,

the silicon nitride comprising region runs entirely along the channel region between the source/drain regions; and

the silicon comprising layer contacts the insulator layer, and the source/drain regions extend to the insulator layer.

6. The circuitry of claim 1 wherein the silicon nitride comprising region has a thickness of from about 10 Angstroms to about 50 Angstroms.

7. Silicon-on-insulator comprising integrated circuitry, comprising:

a substrate comprising an insulator layer of silicon-on-insulator circuitry, the insulator layer comprising silicon dioxide;

a semiconductive silicon comprising layer of the silicon-on-insulator circuitry, the silicon comprising layer being received on the insulator layer, the silicon comprising layer comprising a pair of source/drain regions formed therein and extending to the insulator layer, the silicon comprising layer comprising a partially depleted channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

a silicon nitride comprising region received intermediate the silicon dioxide comprising layer and the source/drain regions and running along at least a portion of the channel region between the source/drain regions.

8. The circuitry of claim 7 wherein the silicon nitride comprising region runs along only a portion of the channel region between the source/drain regions.

9. The circuitry of claim 7 wherein the silicon nitride comprising region runs entirely along the channel region between the source/drain regions.

10. The circuitry of claim 7 wherein the silicon nitride comprising region has a thickness of from about 10 Angstroms to about 50 Angstroms.

11. Silicon-on-insulator comprising integrated circuitry, comprising:

a substrate comprising a semiconductive silicon comprising layer of silicon-on-insulator circuitry, the silicon comprising layer comprising a pair of source/drain regions formed therein and a channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

an insulator layer of the silicon-on-insulator circuitry received on the silicon comprising layer, the insulator layer comprising a first silicon dioxide comprising region in contact with the silicon comprising layer and running along at least a portion of the channel region between the source/drain regions, a silicon nitride comprising region in contact with the first silicon dioxide comprising region and running along at least a portion of the channel region, and a second silicon dioxide comprising region in contact with the silicon nitride comprising region, the silicon nitride comprising region being received intermediate the first and second silicon dioxide comprising regions.

12. The circuitry of claim 11 wherein the silicon nitride comprising region runs along only a portion of the channel region between the source/drain regions.

13. The circuitry of claim 11 wherein the silicon nitride comprising region runs entirely along the channel region between the source/drain regions.

14. The circuitry of claim 11 wherein the silicon nitride comprising region has a thickness of from about 10 Angstroms to about 50 Angstroms.

15. The circuitry of claim 11 wherein the first silicon dioxide comprising region has a thickness of from about 10 Angstroms to about 30 Angstroms.

16. The circuitry of claim 11 wherein the source/drain regions extend to the insulator layer.

17. A method of forming silicon-on-insulator comprising integrated circuitry, comprising:

nitridizing an interface of the silicon comprising layer of silicon-on-insulator circuitry with the insulator layer of the silicon-on-insulator circuitry; and

after the nitridizing, forming a field effect transistor gate operably proximate the silicon comprising layer.

18. The method of claim 17 comprising forming said circuitry by joining a first substrate comprising the silicon comprising layer with a second substrate comprising the insulator layer, the nitridizing comprising nitridizing at least one of the first and second substrates prior to the joining.

19. The method of claim 18 wherein the nitridizing comprises chemical vapor deposition.

20. The method of claim 17 comprising forming said circuitry by joining a first substrate comprising the silicon comprising layer with a second substrate comprising the insulator layer to form a joined substrate, the nitridizing comprising nitridizing after forming the joined substrate.

21. The method of claim 17 wherein the nitridizing comprises ion implanting.

22. The method of claim 17 wherein the nitridizing comprises direct plasma nitridation.

23. The method of claim 17 wherein the nitridizing comprises remote plasma nitridation.

24. The method of claim 17 wherein the nitridation is void of either direct or remote nitrogen containing plasma exposure.

25. A wafer bonding method of forming silicon-on-insulator comprising integrated circuitry, comprising:

nitridizing at least a portion of an outer surface of silicon of a device wafer; and

after the nitridizing, joining the device wafer with a handle wafer.

26. The method of claim 25 further comprising oxidizing at least the nitridized portion prior to the joining.

27. The method of claim 25 comprising forming the integrated circuitry to comprise a silicon-on-insulator field effect transistor.

28. The method of claim 25 wherein the nitridizing comprises ion implanting.

29. The method of claim 25 wherein the nitridizing comprises direct plasma nitridation.

30. The method of claim 25 wherein the nitridizing comprises remote plasma nitridation.

31. The method of claim 25 wherein the nitridizing comprises chemical vapor deposition.

32. The method of claim 25 wherein the nitridation is void of either direct or remote nitrogen containing plasma exposure.

33. A wafer bonding method of forming silicon-on-insulator comprising integrated circuitry, comprising:

nitridizing at least a portion of an outer surface of silicon of a device wafer;

after the nitridizing, joining the device wafer with a silicon dioxide comprising surface of a handle wafer;

forming a pair of source/drain regions separated by a channel region within the silicon, the nitridized portion being received intermediate the source/drain regions and the silicon dioxide comprising surface; and

forming a field effect transistor gate operably proximate the channel region.

34. The method of claim 33 further comprising oxidizing at least the nitridized portion prior to the joining.

35. The method of claim 33 wherein the nitridizing comprises ion implanting.

36. The method of claim 33 wherein the nitridizing comprises direct plasma nitridation.

37. The method of claim 33 wherein the nitridizing comprises remote plasma nitridation.

38. The method of claim 33 wherein the nitridizing comprises chemical vapor deposition.

39. The method of claim 33 wherein the nitridation is void of either direct or remote nitrogen containing plasma exposure.

40. A wafer bonding method of forming silicon-on-insulator comprising integrated circuitry, comprising:

forming silicon dioxide on at least a portion of an outer surface of a handle wafer;

nitridizing at least a portion of an outer surface of the silicon dioxide;

after the nitridizing, joining the handle wafer with an outer surface of a device wafer;

forming a pair of source/drain regions separated by a channel region within the silicon, the nitridized portion being received intermediate the source/drain regions and the silicon dioxide; and

forming a field effect transistor gate operably proximate the channel region.

41. The method of claim 40 wherein the outer surface of the device wafer to which the handle wafer is joined comprises crystalline silicon.

42. The method of claim 40 wherein the outer surface of the device wafer to which the handle wafer is joined comprises silicon nitride.

43. The method of claim 40 wherein the outer surface of the device wafer to which the handle wafer is joined comprises silicon dioxide.

44. The method of claim 40 wherein the nitridizing comprises ion implanting.

45. The method of claim 40 wherein the nitridizing comprises direct plasma nitridation.

46. The method of claim 40 wherein the nitridizing comprises remote plasma nitridation.

47. The method of claim 40 wherein the nitridizing comprises chemical vapor deposition.

48. The method of claim 40 wherein the nitridation is void of either direct or remote nitride containing plasma exposure.

49. A method of forming silicon-on-insulator comprising integrated circuitry, comprising:

forming the silicon comprising layer of the silicon-on-insulator circuitry;

forming a pair of source/drain regions in the silicon comprising layer and a channel region in the silicon comprising layer which is received intermediate the source/drain regions;

forming a transistor gate operably proximate the channel region;

forming the insulator layer of the silicon-on-insulator circuitry, the insulator layer being formed to comprise a first silicon dioxide comprising region in contact with the silicon comprising layer and running along at least a portion of the channel region between the source/drain regions, a silicon nitride comprising region in contact with the first silicon dioxide comprising region and running along at least a portion of the channel region, and a second silicon dioxide comprising region in contact with the silicon nitride comprising region, the silicon nitride comprising region being received intermediate the first and second silicon dioxide comprising regions.

50. The method of claim 49 comprising forming said circuitry by joining a first substrate comprising the silicon comprising layer with a second substrate comprising the insulator layer, forming the silicon nitride comprising region comprising nitridizing at least one of the first and second substrates prior to the joining.

51. The method of claim 50 wherein the nitridizing comprises ion implanting.

52. The method of claim 50 wherein the nitridizing comprises direct plasma nitridation.

53. The method of claim 50 wherein the nitridizing comprises remote plasma nitridation.

54. The method of claim 50 wherein the nitridation is void of either direct or remote nitrogen containing plasma exposure.

55. The method of claim 49 comprising forming said circuitry by joining a first substrate comprising the silicon comprising layer with a second substrate comprising the insulator layer to form a joined substrate, forming the silicon nitride comprising region comprising nitridizing after forming the joined substrate.

56. The method of claim 55 wherein the nitridizing comprises ion implanting.

57. The method of claim 55 wherein the nitridizing comprises direct plasma nitridation.

58. The method of claim 55 wherein the nitridizing comprises remote plasma nitridation.

59. The method of claim 55 wherein the nitridation is void of either direct or remote nitrogen containing plasma exposure.

60. The method of claim 55 comprising forming the silicon nitride comprising region to have a thickness of from about 10 Angstroms to about 50 Angstroms.

61. The method of claim 55 comprising forming the first silicon dioxide comprising region to have a thickness of from about 10 Angstroms to about 50 Angstroms.